Karlsruhe Institute of Technology

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# Spinnaker2 LDPC Decoder

**Bachelor's Thesis/Master's Thesis**

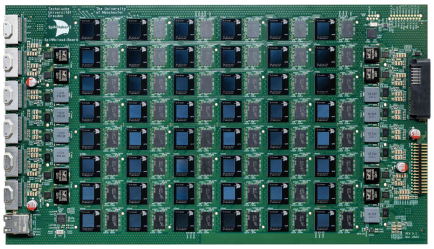
## Project

As global communication demands increase, energy efficiency in communication devices becomes increasingly crucial. A substantial part of a receiver's energy budget is consumed by the decoder for error-correcting codes. A very common class of error-correcting codes is LDPC codes, which are often used with iterative belief propagation decoders.

This thesis will focus on harnessing the innovative technology of SpiNNaker2 chips, inspired by the human brain, to develop an energy-efficient decoder.
The Spinnaker2 architecture consists of 48 chips forming a SpiNNcloud board, which together are equipped with 7,296 sparsely interconnected cores, enabling energy efficiency through dynamic sparsity.

The primary objective is to implement a MINSUM decoder for a single core on a SpiNNaker2 chip, focusing on its energy efficiency.
Additionally, an effective load-balancing mechanism should be designed to optimize the performance and utilization of multiple decoders across the SpiNNcloud board.
A further goal of the project is to utilize the noise generators of the Spinnaker2 chips to create an on-board simulator to assess the decoders' performance in real-time.

Finally, the simulations will be analyzed and evaluated for speed and energy efficiency, and compared with classical decoding architectures.



## Tasks

1. Implementation of a MINSUM decoder on the Spinnaker2 chip
2. Development of a load-balancing mechanism
3. Measurement-based evaluation of the system's performance.

## Requirements

- ✔ Channel Coding
- ✔ C/C++

## Institute

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